INTRODUCTION:
With the degradation of the transistor’s intrinsic gain in CMOS technologies, multistage amplifiers have become increasingly developed in recent years, since they provide high DC gains without sacrificing output swings. Many modern applications require high-gain and fast settling operational transconductance amplifiers (OTAs) driving large capacitive loads in the order of hundreds Ferro farads. In this context the design of high-gain OTAs driving heavy capacitive loads is a difficult task, especially when nanometers technologies are adopted, as they suffer from a drastic reduction of the intrinsic gain. This can be only partially satisfied by the adoption of non-minimum channel length transistors. The design of multistage amplifiers is also complicated. In general, classical topologies based on the nested Miller compensation (NMC) are area/power inefficient and Reversed nested Miller compensation (RNMC) topology causes the high-frequency gain reduction. The single Miller capacitor compensation network consists passive components only and is implemented without using extra transistors, thus saving circuit complexity and power consumption. The last three stages are implemented using the simplest common source stages, thus involving minimum transistors number. Regardless this simplicity, a class AB behavior is achieved, further improved by a slew-rate enhancement (SRE) section that enables large capacitive loads to be driven.

The paper is organized as follows. The compensation techniques and implementation of the circuit are discussed in section II. The simulation results and output values are reported in section III. Finally the conclusion is given in section IV.

CIRCUIT IMPLEMENTATION
The most popular and practical approach is the Miller compensation technique. In this method, a compensation capacitor $C_{C1}$ is placed between the input and output of the fourth stage amplifier. Stability is improved by exploiting the phenomenon of pole splitting. Pole splitting has the effect of pushing one of the two dominant poles to a lower frequency and pushing the other dominant pole to a higher frequency. The pole-splitting principle behind two-stage Miller compensation can be extended to stabilize op amps of more than two horizontal gain stages. A popular multi-stage Miller compensation technique is the nested-Miller compensation (NMC) method. In order to obtain adequate stability margin, the closed-loop bandwidth must be lower than the second pole by a certain factor. Since the $p2$ is near the same frequency as $p1$ of the single-stage op amp, the maximum achievable closed-loop bandwidth of the two-stage op amp will always be lower than that of the single-stage op amp with a first-order transfer function. The settling time of a second-order system is difficult to compute and
predict as it is highly dependent on both its gain-bandwidth product and its phase margin.

**IMPLEMENTATION & SIMULATION RESULTS**

![Proposed Circuit diagram](image1)

**CONCLUSION**

A high-performance four-stage OTA driving 1fF load has been presented. The amplifier uses minimum transistors count, since three gain stages are implemented through the simplest common source configuration, and develops a compensation network made up of a single Miller capacitor with a series resistance and two R-C parallel branches. The design was developed using a 0.13µm CMOS technology. It provides DC gain greater than 45 dB, gain-bandwidth product of about 3 MHz. The proposed amplifier shows better performance as compared to all previously reported four-stage OTAs.

**REFERENCES**


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